What is claimed is:

1. A method of packaging Integrated Circuit devices, comprising:

providing an Integrated Circuit device;

providing a heatsink for said Integrated Circuit device;

providing a substrate on which to mount said Integrated Circuit device;

creating a cavity surrounding said Integrated Circuit device, two surfaces of said cavity comprising said heatsink and said substrate, said cavity comprising a means for entering a molding compound into said cavity;

inserting said Integrated Circuit device into said cavity; and

injecting a molding compound into said cavity.

2. The method of claim 1 wherein said Integrated Circuit (IC) device has a top surface and a bottom surface, contact points to said IC device are mounted in said bottom surface of said device.

3. The method of claim 1 wherein said Integrated Circuit device is selected from a group comprising Ball Grid Array (BGA), Land Grid Array (LGA) and Pin Grid Array (PGA), Chip Scale Packaging (CSP) and Quad Flat Pack (QFP) devices.

4. The method of claim 1 wherein said providing a substrate is providing a means for connecting contact points of said IC device with surrounding electrical circuitry.

5. The method of claim 1 wherein said substrate contains; an upper surface;

electrical contact points provided in said upper surface, forming substrate upper surface contact points, provided to make electrical contact with contact points of said IC device;

a lower surface;

electrical contact points provided in said lower surface, forming substrate lower surface contact points, provided to make electrical contact with surrounding electrical circuitry of which said IC device is a functional component; and

a network of conducting interconnect lines that interconnects said substrate upper surface contact points with said substrate lower surface contact points said network to be contained in one or more planes within said substrate.

6. The method of claim 1 wherein said creating a cavity is:

placing said heatsink in a plane that is parallel to a plane of said substrate;

creating four planer spacers that separate said heatsink from said substrate by a measurable amount, said amount to be selected such that contact points of said IC device make contact with said substrate upper surface contact points while a upper surface of said IC device makes contact with said heatsink; and

forming a cavity, the heatsink and the substrate forming opposite walls of said cavity, said four planer spacers forming two sets of two opposing walls of said cavity, two walls that make up each of these sets of opposing walls being parallel and having identical geometric dimensions, a surface of said heatsink being parallel with a plane of said substrate.

7. The method of claim 1 wherein said creating a cavity is creating a cavity of a size such that one or more IC devices can simultaneously be fitted inside said cavity, creating a molding that contains one or more IC devices.

8. The method of claim 7 wherein a molding that contains more than one IC device is separated into one or more moldings that contain one or more IC devices.

9. The method of claim 1 with the additional step of positioning said inserted Integrated Circuit device with the cavity into which it has been inserted into a mold injection station under control of automatic transport of said IC device.

10. The method of claim 1 with the additional step of exposing said IC device to UV light, curing said molding.

11. The method of claim 1 whereby said heatsink is replaced by a surface of geometric dimensions that are equal to geometric dimensions of said substrate, said surface does not having heat dissipating characteristics of a heatsink.

12. An Integrated Circuit package structure, comprising:

an Integrated Circuit device, having a top surface and a bottom surface, electrical contact points to said IC device are mounted in the bottom surface of said IC device;

a heatsink for said Integrated Circuit device;

a substrate on which to mount said Integrated Circuit device, having a upper surface and a lower surface, points of electrical contact to said IC device having been provided in said upper surface, points of electrical contact for further interconnect of said IC package to surrounding circuitry or components having been provided in said lower surface;

a cavity for inserting said Integrated Circuit device, said cavity to be a closed cavity that encloses said IC device, said cavity being provided with an opening through which a molding compound can be entered into said cavity; and

a molding compound for insertion into said cavity.

13. The Integrated Circuit package structure of claim 12 wherein said Integrated Circuit device is selected from a group comprising Ball Grid Array (BGA), Land Grid Array (LGA) and Pin Grid Array (PGA), Chip Scale Packaging (CSP) and Quad Flat Pack (QFP) devices.

14. The Integrated Circuit package structure of claim 12 wherein said substrate is a means for connecting contact points of said IC device with surrounding electrical circuitry.

15. The Integrated Circuit package structure of claim 12 wherein said substrate comprises;

an upper surface;

electrical contact points in said upper surface, forming substrate upper surface contact points, provided to make electrical contact with contact points of said IC devices;

a lower surface;

electrical contact points in said lower surface, forming substrate lower surface contact points, provided to make electrical contact with surrounding electrical circuitry of which said IC device is a functional component; and

a network of interconnect lines that interconnects said substrate upper surface contact points with said substrate lower surface contact points, said network to be contained in one or more planes within said substrate.

16. The Integrated Circuit package structure of claim 12 wherein said cavity comprises said heatsink, said substrate and four planer spacers that separate said heatsink from said substrate by a measurable amount, said amount to be selected such that contact points of said IC device make contact with said substrate upper surface contact points while a top surface of said IC device makes contact with said heatsink, said heatsink and said substrate forming opposite walls of said cavity while said four spacers form two sets of two opposite walls of said cavity whereby two walls that make up each of these two sets of opposite walls are parallel and have identical geometric dimensions, the surface of said heatsink being parallel with the surface of said substrate.

17. The Integrated Circuit package structure of claim 12 wherein said cavity is a cavity of a size such that one or more IC devices can simultaneously be fitted inside said cavity thereby creating a molding that contains one or more IC devices.

18. The Integrated Circuit package structure of claim 17 wherein a molding that comprises more than one IC device is separated into one or more moldings that contain one or more IC devices.

19. The Integrated Circuit package structure of claim 12 with the addition of a means for positioning said inserted Integrated Circuit device with said cavity into which it has been inserted into a mold injection station under control of automatic transport of said IC device.

20. The Integrated Circuit package structure claim 12 with the addition of a means for exposing said IC device to UV light thereby curing said molding.

21. The Integrated Circuit package structure of claim 12 whereby said heatsink is replaced by a surface of geometric dimensions that are equal to the dimensions of said substrate but whereby said surface does not have heat dissipating characteristics of a typical heatsink.

22. A method of packaging an Integrated Circuit (IC) device, comprising:

providing an Integrated Circuit (IC) device having a flat first surface on which no points of input/output connect are provided for said IC device, having a flat second surface on which points of input/output connect comprising solder bumps or contact balls or contact pads are provided for said IC device;

providing a heatsink having a flat first surface, further having a flat second surface;

mounting said IC device on the fist surface of said heatsink by joining said first surface of said IC device with said first surface of said heatsink, creating a first assembly;

providing an IC substrate having a flat first surface, points of electrical interconnect comprising contact pads or via openings have been provided in or on said first surface, further having a second surface, points of electrical interconnect comprising solder bumps or contact balls or contact pads have been provided in or on said second surface;

mounting said first assembly on said IC substrate by joining said solder bumps or contact balls or contact pads provided in or on said second surface of said IC

device with said points of electrical interconnect provided in said first surface of said IC substrate, creating a second assembly;

providing a cavity for said second assembly, said cavity to comprise four planes that are bordered by said heatsink and said IC substrate and that intersect said first surface of said heatsink and said first surface of said IC substrate under an angle, said cavity further enclosing said Integrated Circuit device, said cavity further having been provided with an opening through which a molding compound can be injected; and injecting said molding compound into said cavity.